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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/972,963	10/10/2001	Gee-Sung Chae	3430-0168P	6251

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BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
WILSON, SCOTT R	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/972,963	CHAE, GEE-SUNG	
	Examiner	Art Unit	
	Scott R. Wilson	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *8-16 and 23-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7 and 17-22* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-7 and 17-22 on 19 May 2003, and further election of the species of claims 1-7 on 11 August 2003 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: THIN FILM TRANSISTOR ARRAY GATE ELECTRODE FOR LIQUID CRYSTAL DISPLAY DEVICE.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 17 recites the limitation "said gate line" on page 28, line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section

122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1, 2, 4, 5 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al.. As to claim 1, Yamazaki et al., Figure 12, discloses a TFT array substrate for use in a liquid crystal display device, the TFT array substrate comprising a gate line (157) arranged in a transverse direction over a substrate, a metallic oxide layer (col. 12, lines 16-18) surrounding the gate line, a data line (172) arranged in a longitudinal direction perpendicular to the gate line over the substrate, and thin film transistors (130), (140), formed near the crossing of the gate and data lines. Yamazaki et al., Figure 3G, further discloses the thin film transistor comprising a gate electrode (25) over the substrate, the gate electrode being extended from the gate line and surrounded by a metallic oxide (col. 12, lines 16-18), a gate insulation layer (Figure 3F, element 41)(col. 12, lines 53-54) on the metallic oxide surrounding the gate electrode, an active layer (171) and an ohmic contact layer (col. 16, lines 47-50) formed on the gate insulation layer, and source and drain electrodes (52) and (53) formed on the ohmic contact layer over the gate electrode, extended from the data line and spaced apart from the source electrode, respectively (col. 13, lines 1-5), a protection layer (44)(col. 13, lines 6 and 7) formed over said thin film transistor, the protection layer having a drain contact hole that exposes part of the drain electrode, and a pixel electrode (43) (col. 13, lines 12-13) formed in a pixel region that id defined by the gate and data lines, the pixel electrode contacting the drain electrode through the drain contact hole. Yamazaki et al., col. 4, lines 31-49, teaches that the gate electrode may have an oxide of the same metal used in the gate formed "around" the gate, or "surrounding" it, both of which are within the scope of having the metal oxide formed under the gate, on opposite sides of the gate and on top of the gate.

As to claim 2, Yamazaki et al., col. 15, lines 1-4, discloses that the gate may comprise tantalum, titanium or tungsten, which would form a surrounding oxide layer of tantalum oxide, titanium oxide or tungsten oxide, respectively, according to the teachings of col. 4, lines 31-49.

As to claim 4, Yamazaki et al., Figure 3A, discloses (col. 8, lines 64-65) a blocking layer, or buffering layer formed between the substrate (1) and the gate line and gate electrode (25) and (26).

As to claim 5, Yamazaki et al., col. 15, lines 1-4, discloses that the gate may comprise tantalum, titanium or tungsten, which would form a surrounding oxide layer of tantalum oxide, titanium oxide or tungsten oxide, respectively, according to the teachings of col. 4, lines 31-49. Yamazaki et al. discloses (col. 8, line 64), however, that the blocking film (24) of Figure 3A, is formed of silicon oxide.

As to claim 7, Yamazaki et al. discloses (col. 8, line 64) that the blocking film (24) of Figure 3A is formed of silicon oxide.

Claims 17-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al.. As to claim 17, Yamazaki et al., Figures 3A through 3G and 12, discloses an insulated conductor structure for use in a TFT array substrate of a liquid crystal display device, the conductor structure comprising a substrate (1), a metallic conductive line (157) arranged over said substrate, a metallic conductive electrode (25) and (26) arranged over said substrate and branching off said conductive line, a metallic oxide layer (col. 12, lines 16-18) surrounding said electrode and an insulation layer (41) on said conductive line and said metallic oxide layer.

As to claim 18, Yamazaki et al., col. 15, lines 1-4, discloses that the conductor structure, embodied as a gate, may comprise tantalum, titanium or tungsten, which would form a surrounding oxide layer of tantalum oxide, titanium oxide or tungsten oxide, respectively, according to the teachings of col. 4, lines 31-49.

As to claim 19, Yamazaki et al., Figure 3A, discloses (col. 8, lines 64-65) a blocking layer, or buffering layer formed between the substrate (1) and the conductive line and conductive electrode, embodied as a gate line and gate electrode (25) and (26).

As to claim 20, Yamazaki et al. discloses (col. 8, line 64) that the blocking film (24) of Figure 3A is formed of silicon oxide.

As to claim 21, Yamazaki et al. embodies the conductor structure of claim 17 as a gate line and gate electrode (col. 15, lines 16-17).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. in view of Dimitrakopoulos et al.. Yamazaki et al. discloses the invention of claim 2, as described above. Yamazaki et al. does not disclose expressiy the gate line and gate electrode formed from copper. Dimitrakopoulos et al., Claim 5, discloses the gate electrode of a thin film transistor comprised of copper. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the gate electrode of Yamazaki et al. from copper. The motivation for doing so would have been to take advantage of the superior conductivity characteristics recognized for copper. Therefore, it would have been obvious to combine Dimitrakopoulos et al. with Yamazaki et al. to obtain the invention as specified in claim 3.

Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. in view of Dimitrakopoulos et al.. Yamazaki et al. discloses the invention of claim 17, as described above. Yamazaki et al. does not disclose expressly the conductive line and conductive electrode formed from copper. Dimitrakopoulos et al., Claim 5, discloses the gate electrode of a thin film transistor comprised of copper. At the time of invention, it would have been obvious to a person of ordinary skill in the art to form the conductive electrode of Yamazaki et al. from copper. The motivation for doing so would have been to take advantage of the superior conductivity characteristics recognized for copper. Therefore, it would have been obvious to combine Dimitrakopoulos et al. with Yamazaki et al. to obtain the invention as specified in claim 22.

Allowable Subject Matter

Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No prior art discloses a tantalum nitride or titanium nitride blocking layer formed under a gate electrode surrounded by a metallic oxide in a TFT.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott R. Wilson whose telephone number is 703-308-6557. The examiner can normally be reached on M-F 8:30 - 4:30 Eastern.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.

srw
October 16, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800